



is pleased to invite you to the Summer School on

# Nanoelectronic Circuits and Tools

14-18 July 2008  
EPFL Auditorium CO3

This summer school is partly sponsored by the Materials for Micro and Nano Systems (MMNS) Education and Research unit of the CCMX Competence Centre for Materials Science and Technology. All lectures will take place at EPFL in Auditorium CO3.

Registration fee is **150 CHF** and it includes daily lunch at an on-campus restaurant and two coffee breaks per day during the week of the summer school. On-line registration is required. Please see <http://si.epfl.ch/page12409.html> for abstracts, and registration.

Morning session: Nanoscale Electronics (10:00 – 12:15)		
Date:	Lecturer:	Schedule:
Monday 14 July	<b>H.-S. Philip Wong</b> <i>Stanford University</i>	10:00–11:00 Beyond CMOS Scaling – What's Next? 11:00–11:15 <i>Coffee break</i> 11:15–12:15 The Future of CMOS Scaling
Tuesday 15 July	<b>Shunri Oda</b> <i>Tokyo Institute of Technology</i>	10:00–11:00 Silicon quantum dots: the future of electronics and photonics? 11:00–11:15 <i>Coffee break</i> 11:15–12:15 Novel Nano–ElectroMechanical–System Devices
Wednesday 16 July	<b>Ken Uchida</b> <i>Tokyo Institute of Technology</i>	10:00–11:00 Classical versus Ballistic Transports 11:00–11:15 <i>Coffee break</i> 11:15–12:15 Performance Booster Technologies for Advanced MOSFETs: Stress Engineering and Surface Orientations other than (001)
Thursday 17 July	<b>Kaustav Banerjee</b> <i>UC Santa Barbara</i>	10:00–11:00 Carbon Nanotube Interconnects for Next Generation ICs– Part I 11:00–11:15 <i>Coffee break</i> 11:15–12:15 Carbon Nanotube Interconnects for Next Generation ICs– Part II
Friday 18 July	<b>Gianfranco Cerofolini</b> <i>University of Milano–Bicocca</i>	10:00–11:00 Silicon in vivo—Linking the world of micro–electronics to that of living systems 11:00–11:15 <i>Coffee break</i> 11:15–12:15 A roadmap to nanobio–sensing
Afternoon session: Computer Aided Design (14:00 – 16:15)		
Date:	Lecturer:	Schedule:
Monday 14 July	<b>Dennis Sylvester</b> <i>University of Michigan</i>	14:00–15:00 Pushing Nanoscale CMOS: Design–related Challenges 15:00–15:15 <i>Coffee break</i> 15:15–16:15 Extending Nanoscale CMOS: Analyze, Sense, Correct, and Exploit
Tuesday 15 July	<b>Massoud Pedram</b> <i>University of Southern California</i>	14:00–15:00 Minimizing Leakage Power in CMOS: Technology Issues 15:00–15:15 <i>Coffee break</i> 15:15–16:15 Minimizing Leakage Power in CMOS: Design Optimization Techniques
Wednesday 16 July	<b>Jason Cong</b> <i>UCLA</i>	14:00–15:00 Design for Nanotechnologies and 3D ICs 15:00–15:15 <i>Coffee break</i> 15:15–16:15 Thermal–Aware 3D IC Physical Design and 3D Architecture Exploration
Thursday 17 July	<b>Subhasish Mitra</b> <i>Stanford University</i>	14:00–15:00 Carbon Nanotube Transistor Circuits: Opportunities, Challenges, and Experimental Demonstration 15:00–15:15 <i>Coffee break</i> 15:15–16:15 Imperfection–Immune Carbon Nanotube VLSI Logic Circuits
Friday 18 July	<b>Pol Marchal</b> <i>IMEC</i>	14:00–15:00 A roadmap for 3D Technologies and their design Opportunities 15:00–15:15 <i>Coffee break</i> 15:15–16:15 Path Finding – a design/ technology co–exploration